COL



plicants:

Christian FRAISSE and Claude RENOUS

Serial No:

09/690,634

Patent No. 6,928,158 B1

Filed:

October 17, 2000

Issued: August 9, 2005

For:

TRANSMISSION OF A CLOCK BY CAPACITIVE

ISOLATING BARRIER

Examiner:

Alexander Jamal

Art Unit:

2643

Confirmation, No.:

1622

Certificate

ATTN: Certificate of Correction Branch

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

AUG 2 4 2005

of Correction

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction

[X] Copies of: Page 5 of Apl as Filed and Cols 3 and 4 of U.S. Patent No. 6,928,158

[X] PTO Form SB/44

[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617) 646-8000, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 on August 2005.

Attorney Docket No.: S1022.80429US00

<u>XNDD</u>

Respectfully submitted,

Christian Fraisse et al., Applicant

James H. Morris

Reg. No.: 34,681

WOLF, GREENFIELD & SACKS, P.C.

600 Atlantic Avenue

Boston, Massachusetts 02210

Tel. (617) 646-8000





IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

Christian FRAISSE and Claude RENOUS

Serial No:

09/690,634

Patent No. 6,928,158 B1

Filed:

October 17, 2000

Issued: August 9, 2005

For:

TRANSMISSION OF A CLOCK BY CAPACITIVE

ISOLATING BARRIER

Examiner:

Alexander Jamal

Art Unit:

2643

Confirmation. No.:

1622

ATTN: Certificate of Correction Branch

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

Sir/Madam:

Patentees respectfully request the correction of errors found in the above-captioned patent. Specifically, there are typographical errors in columns 3 and 4 of U.S. Patent No. 6,928,158 B1.

Below claim 6 as they appear in column 3, line 51 through column 4, line 7 of U.S. Patent No. 6,928,158.

In conventional systems, such disturbances cause a phase inversion of the clock restored on the line side. Now, when clock signal CK' correctly restores signal CK, the shape of signal Tx+ is recovered. However, if the phase of signal CK' is inverted with respect to signal CK, for example, due to a parasitic disturbance p (FIG. 4D), the restored signal T'x+ then is in phase opposition with respect to signal Tx+. The modem that notices the error by checking algorithms must then reposition its demodulator on the new **phases** relation (the involved demodulator is that, not shown, of the actual modem, downstream of the receive head, and not the demodulator associated with the isolation barrier). Now, each disturbance of the modem reception causes a decrease of the transmission level to enable the modem algorithms to correct the received data. Further, once a modem has switched to a lower transmission level, it does not recover by itself to a better level until the end of the communication.

In conventional systems, the initial state of the regeneration circuit most often is random. It is thus possible to be, as soon as the beginning of a communication, in clock phase opposition. In this case, the modem already

Serial No. 09/690,634 - 2 - Art Unit: 2643

Confirmation. No.: 1622

switches to a first lower level. If, afterwards, during the communication, a new parasitic pulse occurs, the modem switches to row a still lower level, due to the new clock phase inversion. (Emphasis added)

Below claim 6 as they appear on page 5 of the application as filed.

In conventional systems, such disturbances cause a phase inversion of the clock restored on the line side. Now, when clock signal CK' correctly restores signal CK, the shape of signal Tx+ is recovered. However, if the phase of signal CK' is inverted with respect to signal CK, for example, due to a parasitic disturbance p (FIG. 4D), the restored signal T'x+ then is in phase opposition with respect to signal Tx+. The modem that notices the error by checking algorithms must then reposition its demodulator on the new **phase** relation (the involved demodulator is that, not shown, of the actual modem, downstream of the receive head, and not the demodulator associated with the isolation barrier). Now, each disturbance of the modem reception causes a decrease of the transmission level to enable the modem algorithms to correct the received data. Further, once a modem has switched to a lower transmission level, it does not recover by itself to a better level until the end of the communication.

In conventional systems, the initial state of the regeneration circuit most often is random. It is thus possible to be, as soon as the beginning of a communication, in clock phase opposition. In this case, the modem already switches to a first lower level. If, afterwards, during the communication, a new parasitic pulse occurs, the modem switches to a still lower level, due to the new clock phase inversion. (Emphasis added)

No amendments were made by either the Examiner or Applicants to change "phase" to "phases" on page 5, line 2 of the application as filed (column 3, line 59 of U.S. Patent No. 6,928,158) or to change "to a" to "to row a" on page 5, lines 12-13 of the application as filed (column 4, line 6 of U.S. Patent No. 6,928,158).

Support for the requested corrections can be found in enclosed, highlighted copy of page 5 of the application as filed and columns 3 and 4 of U.S. Patent No. 6,928,158. Also enclosed is PTO form SB/44.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

Serial No. 09/690,634

Confirmation. No.:

- 3 -

Art Unit: 2643

Patentees respectfully submit that, since the errors for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a

fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No.

23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

1622

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 on August

Attorney Docket No.: S1022.80429US00

XNDD

Respectfully submitted,

Christian Fraisse et al., Applicant

James H. Morris

Reg. No.: 34,681

WOLF, GREENFIELD & SACKS, P.C.

600 Atlantic Avenue

Boston, Massachusetts 02210

Tel. (617) 646-8000

UNITED STATES PATENT AND TRADEMARK OFFICE **CERTIFICATE OF CORRECTION**

PATENT NO. :

6,928,158 B1

DATED

August 9, 2005

INVENTOR(S):

Christian Fraisse and Claude Renous

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Line 59 of col. 3 should read:

-- then reposition its demodulator on the new phase relation--

Line 6 of col. 4 should read:

-- a new parasitic pulse occurs, the modem switches to row a--

MAILING ADDRESS OF SENDER

PATENT NO. 6,928,158

James H. Morris Wolf, Greenfield & Sacks, P.C. 600 Atlantic Avenue Boston, Massachusetts 02210 AUG 2 5 2005

4

On the receive side, modulator 32 that provides signals Sr+ and Sr- to capacitors C3 and C4 receives the received signals R'x+ and R'x- in the baseband from an amplifier 35, the respective inputs of which are, like the outputs of amplifier 33, connected to a duplexer 36 (4W/2W), the function of which is to perform a 4 wire-2 wire conversion. Circuit 36 generally includes echo cancellation means for eliminating, from the signal received from the line, the echo of the transmitted signal to enable a good reception. The telephone line has been symbolized by its two conductors 10 TIP and RING at the output of duplexer 36.

The operation of an interface system such as illustrated in FIGS. 1 to 3 is known and will not be explained in detail. Only the elements to which the present invention applies, that is, more specifically, the clock transmission through 15 isolation barrier 1, will be reviewed.

FIGS. 4A, 4B, 4C, 4D, and 4E schematically illustrate, in the form of timing diagrams, the clock transmission problem that the present invention aims at solving. FIG. 4A shows an example of a baseband signal meant to cross isolation barrier 1. For simplification, no account will be taken of the differential structure of the signals and only one useful signal has been shown in FIG. 4A. It may be any of signals Tx+, Tx-, R'x+, R'x-. For example, it is assumed that it is signal Tx+ referenced with respect to the common mode voltage 25 VCM of the equipment.

FIG. 4B shows clock signal CK used for the modulation. The signal has been shown as being referenced with respect to common mode voltage VCM due to the multiplication by 1 and -1 effected by the modulator.

FIG. 4C illustrates the shape of signal St+obtained at the output of modulator 21. This signal includes rectangular pulses at the frequency of clock signal CK in an envelope formed with signal Tx+ and its inverse.

FIG. 4D shows an example of the shape of clock signal CK' recovered on the side of circuit 3. FIG. 4E shows the shape of signal Tx+ recovered at the output of demodulator 31. The demodulation is performed, like the modulation, by a multiplying by 1 or -1 by means of the clock signal, here by a multiplying of signal St+ by signal CK'.

An example of interface to which the present invention more specifically applies is described in U.S. Pat. No. 5,500,895, the content of which is incorporated in the present description by express reference.

A problem that is raised in the type of interface system has to do with disturbances that may affect clock signal CK' and that originate from radioelectric disturbances due, for example, to electric household appliances (for example, the starting of a motor or of a compressor of a refrigerator).

In conventional systems, such disturbances cause a phase inversion of the clock restored on the line side. Now, when clock signal CK' correctly restores signal CK, the shape of signal Tx+ is recovered. However, if the phase of signal CK' is inverted with respect to signal CK, for example, due to a 55 parasitic disturbance p (FIG. 4D), the restored signal Tx+ then is in phase opposition with respect to signal Tx+. The modem that notices the error by checking algorithms must then reposition its demodulator on the new phases relation (the involved demodulator is that, not shown, of the actual 60 modem, downstream of the receive head, and not the demodulator associated with the isolation barrier). Now, each disturbance of the modem reception causes a decrease of the transmission level to enable the modern algorithms to correct the received data. Further, once a modem has 65 switched to a lower transmission level, it does not recover by itself to a better level until the end of the communication.

In conventional systems, the initial state of the regeneration circuit most often is random. It is thus possible to be, as soon as the beginning of a communication, in clock phase opposition. In this case, the modem already switches to a first lower level. If, afterwards, during the communication, a new parasitic pulse occurs, the modem switches to row a still lower level, due to the new clock phase inversion.

It should be noted that processing circuit 3, on the line side, performs other functions than those illustrated in FIG. 3. In particular, this circuit is used to detect the presence of a ringing and to detect a standardized line impedance (for example, on the order of 600 ohms). In certain cases, other capacitors are used in the isolation barrier to transmit other types of signals.

SUMMARY OF THE INVENTION

The present invention aims at overcoming the disadvantages of known capacitive isolation interface systems.

The present invention more specifically aims at providing a novel solution to enable a synchronous regeneration of a high-frequency modulation clock by a processing circuit on the line side.

The present invention also aims at providing a solution that is compatible with the rest of the functions of conventional interface circuits and, in particular, with a caller identification function during the ringing period.

A first solution that comes to mind would be to use a phase-locked loop (PLL) to obtain a correct clock on the line side. Such a solution must however be discarded, since a phase-locked loop would not detect a transient disturbance causing the phase inversion. Further, this solution would be particularly complex to implement.

It should be noted that the present invention aims at avoiding a phase inversion due to a random disturbance in the clock signal transmission and not at avoiding any phase shift between clock CK' on the line side and clock CK on the equipment side. Indeed, there necessarily is a slight phase shift between these clocks, which will not be taken into account and which is not disturbing as long as this phase shift is approximately regular, which is the case most of the time since it is a phase shift due to physical propagation times. Further, it may be provided, as for example in above-mentioned U.S. Pat. No. 5,500,895, to take account of the delays between logic layers of the system for the clock signal transmission (element 117, FIG. 6).

Another solution would be, if it was possible, to use software means to differentiate random disturbances due to the starting of an electric appliance from disturbances due to the line. Indeed, when dealing with line disturbances, it is normal for the modem to switch to a lower transmission level, while this is not justified in the case of a transient parasitic disturbance. However, nothing enables detecting the origin of the disturbance on the modem side, so that such a software solution would not be satisfactory.

The present invention originates from a novel analysis of the phenomena that cause the phase inversion problem of the regenerated clock signal on the line side. For the present inventors, this problem is due to the circuit used for this regeneration.

FIG. 5 shows a conventional example of a clock regeneration circuit 34 downstream of an isolation barrier 1 of an interface system between a telephone line and a modem. In FIG. 5, only circuit 34 has been shown, with capacitors C5 and C6 of transmission barrier 1 that transmit signals CK+ and CK- coming from block 24 (FIG. 1). To simplify, it is

signal T'x+ then is in phase opposition with respect to signal Tx+. The modem that notices the error by checking algorithms must then reposition its demodulator on the new phase relation (the involved demodulator is that, not shown, of the actual modem, downstream of the receive head, and not the demodulator associated with the isolation barrier). Now, each disturbance of the modem reception causes a decrease of the transmission level to enable the modem algorithms to correct the received data. Further, once a modem has switched to a lower transmission level, it does not recover by itself to a better level until the end of the communication.

5

10

15

20

25

In conventional systems, the initial state of the regeneration circuit most often is random. It is thus possible to be, as soon as the beginning of a communication, in clock phase opposition. In this case, the modem already switches to a first lower level. If, afterwards, during the communication, a new parasitic pulse occurs, the modem switches to a still lower level, due to the new clock phase inversion.

It should be noted that processing circuit 3, on the line side, performs other functions than those illustrated in Fig. 3. In particular, this circuit is used to detect the presence of a ringing and to detect a standardized line impedance (for example, on the order of 600 ohms). In certain cases, other capacitors are used in the isolation barrier to transmit other types of signals.

Summary Of The Invention

The present invention aims at overcoming the disadvantages of known capacitive isolation interface systems.

The present invention more specifically aims at providing a novel solution to enable a synchronous regeneration of a high-frequency modulation clock by a processing circuit on the line side.

The present invention also aims at providing a solution that is compatible with the rest of the functions of conventional interface circuits and, in particular, with a caller identification function during the ringing period.

A first solution that comes to mind would be to use a phase-locked loop (PLL) to obtain a correct clock on the line side. Such a solution must however be discarded, since a phase-locked loop would not detect a transient disturbance causing the phase inversion. Further, this solution would be particularly complex to implement.